In the Claims:

1. (Original) A semiconductor device comprising:

a semiconductor substrate;

a first isolation layer on the semiconductor substrate;

a second isolation layer on the semiconductor substrate, wherein the second isolation layer is spaced apart from the first isolation layer to define a first active region therebetween;

a third isolation layer on the semiconductor substrate, wherein the third isolation layer is spaced apart from the second isolation layer to define a second active region therebetween, and wherein the first, second and third isolation layers define a row;

a first cell gate on the first active region, the first cell gate comprising a first gate dielectric layer, a first storage node, a first multiple tunnel junction barrier and a first source layer that are sequentially stacked;

a second cell gate on the second active region, the second cell gate comprising a second gate dielectric layer, a second storage node, a second multiple tunnel junction barrier and a second source layer that are sequentially stacked;

a first control line surrounding at least a portion of each sidewall of the first cell gate;

a second control line surrounding at least a portion of each sidewall of the second cell gate, the second control line disposed parallel to the first control line;

a first dielectric layer interposed between the first control line and the sidewalls of the first cell gate;

a second dielectric layer interposed between the second control line and the sidewalls of the second cell gate; and

a data line connecting to the first and second cell gates.

2. (Original) The semiconductor device of Claim 1, wherein a first side of the first cell gate overlaps a portion of the first isolation layer and a second side of the first cell gate overlaps a portion of the second isolation layer, and wherein a first side of the second cell gate overlaps a portion of the second isolation layer and a second side of the second cell gate

overlaps a portion of the third isolation layer.

3. (Original) The semiconductor device of Claim 1, further comprising a fourth isolation layer and a fifth isolation layer on the semiconductor substrate, wherein the fourth isolation layer and the fifth isolation layer are parallel to the row defined by the first, second and third isolation layers and wherein the first, second and third isolation layers are positioned between the fourth isolation layer and the fifth isolation layer.

4. (Original) The semiconductor device of Claim 3, wherein the first control line and the second control line cross over the fourth isolation layer and the fifth isolation layer and wherein the data line crosses over the first, second and third isolation layers.

5. (Original) The semiconductor device of Claim 1, further comprising a first spacer interposed at least partially between the first dielectric layer and the first control line and a second spacer interposed at least partially between the second dielectric layer and the second control line.

6. (Original) The semiconductor device of Claim 5, wherein the first spacer and the second spacer comprise polysilicon spacers.

7. (Original) The semiconductor device of Claim 1, wherein a top surface of the first control line is lower than a top surface of the first source layer and wherein a top surface of the second control line is lower than a top surface of the second source layer.

8. (Original) The semiconductor device of Claim 1, further comprising a third dielectric layer between the data line and the top surface of the first and second control lines.

9. (Original) The semiconductor device of Claim 1, wherein a top surface of the first control line is higher than a top surface of the first source layer and wherein a top surface of the second control line is higher than a top surface of the second source layer, and wherein the device further comprises an insulation spacer between the first and second control lines and

the data line.

10. (Original) The semiconductor device of Claim 9, wherein the insulation spacer is formed of one material selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride and aluminum oxide.

11. (Original) The semiconductor device of Claim 5, further comprising a low-concentration impurity-doped region in the semiconductor substrate under both the first spacer and the second spacer and a high-concentration impurity-doped region in the semiconductor substrate under both the first control line and the second control line.

12. (Original) A semiconductor device comprising:

a semiconductor substrate;

a plurality of parallel, spaced apart first isolation layers on the semiconductor substrate;

a plurality of second isolation layers interposed between adjacent ones of the plurality of first isolation layers;

a plurality of rows of cell gates, wherein the rows of cell gates are perpendicular to the plurality of first isolation layers, and wherein each cell gate in the rows of cell gates is on at least a portion of two of the plurality of second isolation layers;

at least one dielectric layer on the sidewalls of the cell gates in the plurality of rows of cell gates;

a plurality of parallel control lines that cross over the plurality of first isolation layers, wherein each of the plurality of control lines surrounds the dielectric layer that is on the sidewalls of each cell gate in a row of the rows of cell gates that corresponds to the control line; and

a plurality of data lines that are parallel to the plurality of first isolation layers, wherein each of the plurality of data lines connects to a subset of the plurality of cell gates.

13. (Original) The semiconductor device of Claim 12, wherein each cell gates

comprises a gate dielectric layer, a storage node, a multiple tunnel junction barrier and a source layer that are sequentially stacked.

14. (Original) The semiconductor device of Claim 13, wherein the data lines connect to a top surface of the cell gates.

15. (Original) The semiconductor device of Claim 12, further comprising a peripheral circuit region in the semiconductor substrate, the peripheral circuit region comprising:

a third isolation layer defining an active region in the semiconductor substrate;

a peripheral gate on the active region and on a portion of the third isolation layer; and

a peripheral gate contact plug electrically connecting to the peripheral gate.

16. (Original) The semiconductor device of Claim 15, wherein the peripheral gate comprises a gate dielectric layer, a storage node, a multiple tunnel junction barrier and a source layer sequentially stacked on the semiconductor substrate.

17. (Original) The semiconductor device of Claim 15, wherein the peripheral gate contact plug is directly connected to the storage node.

Claims 18-38 (Canceled)